VErsatile RAdar – RFSoC based radar demonstrator for multiple applications

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***Abstract*—The Norwegian Defence Research Establishment (FFI) VeRa (Versatile Radar) is a radar demonstrator for multiple applications based on the 1st generation Xilinx RF System on Chip (RFSoC). This paper describes the hardware and software solution, and show results from wideband polarimetric measurements of sea-vessel, land target, and also Synthetic Aperture Radar (SAR) measurements. Finally, planned future developments to make use of the RFSoC flexibility and versatility to improve the sensor are discussed.**

I. Introduction

The radar group at the Norwegian Defense Research Establishment (FFI) has developed a number of radars and radar instrumentation systems. The perhaps most notable of these is the RIMFAX ground-penetrating radar of the MARS-rover [1], but other systems like the BirdRad [2], the HUBRA [3] and the USRP-based cognitive radar [4] show different classes of systems ranging from low-level hardware development through to Software-Defined-Radio (SDR) systems. Radio Frequency System on Chip (RFSoC) systems, altough used in many present developments, have only been published by FFI in radar-related use for digital television based Passive Radar [5].

A close cousin of the Xilinx RFSoC, the MultiProcessor System on Chip (MPSoC), is used in several FFI-designed systems for electronic support (ES), where one of these is the LINE EW-UAS. Further developments of this flexible chip has led to the NORSat-3 payload with navigation radar detector, and soon also the MilSpace2 spectrum monitoring dual satellite system. The MPSoC offers most of the features of the RFSoC, altough the Digital-to-Analog Converter (DAC) and analog-to-digital converter (ADC) needs to be externally connected for Radio Frequency (RF) connectivity. Migrating an ES design onto the RFSoC is therefore a non-complex task, and combining radar and ES is now a priority in the FFI RF group.

The RFSoC is not a particularly new idea. One could for example mention the Chipcon (now Texas Instruments) CC1000-series of chips introduced in 2002, where a transceiver for up to 1GHz was incorporated. These were embedded systems, where the bandwidt was low and the design was for very low power. From those times, all aspects of the RF components have increased in rates and fidelity. The Analog to Digital Converters ADC have markedly increased in sampling rates and resolution, and in the same manner also the Digital to Analog Converters DAC. High quality commercial ADCs suitable for radars can now have 16 bit of resolution and 1 GSps, and reducing to 14 bits of resolution increases the rates to 5GSps and above. ADCs of 14 bits resolution are available at e.g. 12GSps. Due to the Nyquist theorem and aliases, RFSoC systems can work directly on RF at high frequencies, at least up to 6-7 GHz and probably beyond.

On the digital side, the Field-Programmable Gate-Arrays Field-Programmable Gate Array (FPGA) and general purpose processing cores have increased tremendously in processing power, and the data buses and random-access-memory Random Access Memory (RAM) have increased in transfer bandwidths. What has happened in the later years, is a success in packing all these technologies together in a designer-friendly suite where the power and flexibility can be taken to use. Packing powerful processing with multiple channels of DACs and ADCs onto a single chip can ease or enable several key points: fast reconfiguration, design flexibility, lower power usage, smaller footprint, digital beamforming, and also multiple RF sensor domains working in parallell (Multifunction RF). The RFSoC in combination with the high sampling rates therefore offers an intriguing package for the RF engineer.

Several publications now emerge about systems using RFSoCs. [6] show digital beamforming using direct conversion at 28 GHz using the Xilinx RFSoC, and [7] discusses cost reduction of phased array radars through the use of commercial RFSoCs. [8] looks into techniques for calibration of digital beamforming radars by near-field calibration, which will be equally important for these radars as for the analog beamforming systems. Usage of RFSoC is also emerging for radio systems, where e.g. [9] mentions a frequency hopping orthogonal frequency division multiplexing (OFDM) system based on the Xilinx ZCU111 evaluation board.

Multifunction RF is the integration of many RF sensor functions into an integrated package, and in the military RF aspect it is commonly radio, radar and electronic warfare (EW) suits sharing the same RF system. This has been in development, particularly by the US Navy for now several decades, driven by the many RF systems competing for space on the naval ships and at the same time as the demand for signature reduction is increasing. [10] very well describe the recent developments and difficulties on succeeding with Multifunction RF systems, and it is easy to understand the possibilities the RFSoC can have here. The large FPGA of the RFSoC can fit many radio systems in parallell, and the large

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bandwidth of the DAC and ADCs can allow several frequency bands to be used fully in parallel. Also, the single-chip design makes very fast reconfigurations possible.

The radar design described here takes aim at being one of several RF systems within the same chip/design. It has been tested as a monostatic range-Doppler radar, as well as for Synthetic Aperture Radar use. We will describe the hardware integration of the system, the software backend, and finally also show some results from data collected during field measurements.

II. Hardware

The VErsatile RAdar (VERA) system consists of three parts: RF front-end, FPGA and host computer. This section will describe the first two. The host computer consists of a off-the-shelf workstation, hence, the part describing the host computer will be in the software section.

A. RFSoC FPGA design

The VERA system is centered around the Xilinx ZCU111 evaluation board, containing the first generation of RFSoC from Xilinx. The chip contains a FPGA, 4 ARM cores for general purpose programming, two real-time ARM cores, 4 GB of RAM for the ARM-cores and 4 GB of RAM for the FPGA which is also accessible from the ARM cores. Among many interfaces available, VERA can use one or two of the SFP+ connectors for 10Gb ethernet to a host computer. Most importantly, it has 8 ADCs capable of 12-bit resolution and 4.096 GSps and 8 DACs capable of 14-bits resolution and 6.554 GSps. These DACs and ADCs can be synchronized, which in the future will enable digital beam-steering of the antenna.

The VERA system presently use 2 channels of the DACs and ADCs, to enable polarimetric measurements. The system has a direct-RF design where no analog tuning is used. A high-selectivity RF cavity-filter with a passband between 3.1-3.5 GHz is used to suppress out-of-band interference. The ADC sampling rate used is 4.096 GSps, so that the whole band of interest is covered within the 2nd Nyquist zone. Likewise, an equal DAC sampling rate is used for radar signal generation, so that a waveform can be generated on the chip for the entire band of interest. Pulse-by-pulse frequency hopping or several fast interleaved waveforms can be used in future developments, but a non-linear Frequency Modulated (FM) pulse of 280 MHz bandwidth is used now because of VERAs main purpose as a high range-resolution radar. The FPGA block diagram can be seen in Figure 1. The design is using only 2% of the Lookup Table (LUT) and 1% of the Flip-Flops (FF) of the FPGA, as little processing is performed there before transfer to the host computer. 11% of Block-RAM (BRAM) is used for First-in First-out (FIFO) buffer and waveform storage, and 10% of UltraRAM (URAM) is used for buffers to allow transfer of a selected range-area of high range-resolution data to the host. This leaves room for both increasing the complexity of the radar-design, and incorporating ES functionality to create a multifunction RF system.

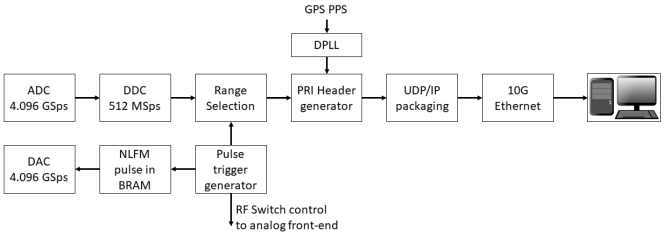

Figure 1. VERA FPGA system block diagram

Originally the radar was envisioned to use pulses with even higher bandwidths. However, the military frequency band of 3.1-3.5 GHz was recently limited to 3.1-3.4 GHz to allow for higher mobile data bandwidths. Therefore, the original bandwidth of 400 MHz which was planned was changed, which was a quick reprogramming of the system. Further in Figure 1, a digital down-conversion on the FPGA is used to convert the original 4 GSps to 512 MSps of complex data. This is done using the built-in down-conversion stage on the Xilinx RF Data converter system. The data rate at this stage is 32.8 Gbps, too high to transfer on one or two 10 Gbps links to the processing computer. The data rate is therefore reduced by selecting an area in range which is to be transferred. The pulse trigger restarts a counter, and a Pulse Repetion Frequency (PRI) header is generated containing time offset from a GPS Pulse-per-Second (PPS) and a second-counter. The PPS is controlled by a Discrete-time or Digital Phase-Locked Loop (DPLL), and the FPGA code for this has been developed by Michael A. Morris [11]. The header is transferred as the first 4 data bytes marking the start of the PRI, and following that the complex sample data from the two reception channels is transferred.

As the previous radars developed by FFI have been real-time capable using Central Processing Unit (CPU) and General Purpose Graphical Processing Units (GPGPU), it has been a conscious design choice to do as little signal processing on FPGA as possible. The flexibility of algorithmic redesign and debugging has shown itself much higher on a host computer rather than on FPGA, but the pulse compression may possibly be shifted to the FPGA in other designs. The biggest hurdle in this design to enable this is the large number of samples on the wide bandwidth pulse, which is too large to fit inside the available Finite Impulse-Response (FIR) filters.

The signal generation is handled by using a pre-generated Non-Linear Frequency Modulation (NLFM) pulse stored in BRAM. A continually cycling pulse-trigger generator is working at a constant pulse repetition frequency (PRF), and at transmission of the pulse, it will also control the RF switches in the front-end while marking the start of reception of the data from the DAC. This very simple design will in the future be modified to also support a variable PRF. While real-time generation of Linear Frequency Modulation (LFM) pulses of varying bandwidth and pulse lengths is fairly easy, programmatical generation of NLFM pulses has not yet been

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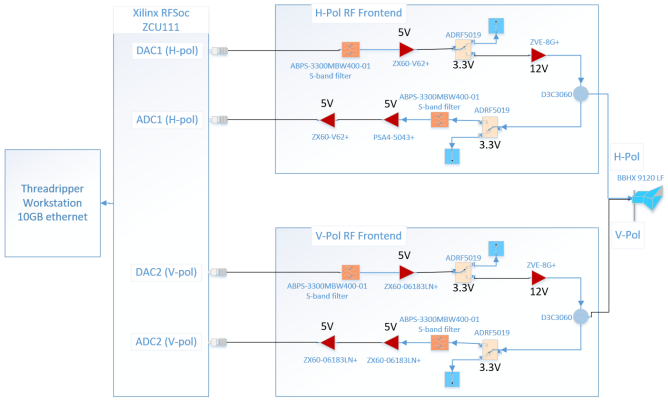

Figure 2. VERA RF front-end block diagram

implemented on FPGA. If implemented, this can in the future create more flexibility in the radar while saving BRAM.

B. VERA RF front-end

The VERA system is a wideband dual-polarized radar system in S-band and, hence, the RF front-end must reflect this. Figure 2 is a block diagram of the system, with two parallel RF paths for the two polarizations.

The transmitter path consist of the following elements (in order):

- Amp.: Mini Circuits ZX60-V62+, 15.5 dB gain, 5.1dB noise factor (NF).
- RF Filter: AWG ABPF-3300MBW400-01, 0.8 dB insertion loss (IL).
- RF Switch: Analog Devices ADRF5019, 0.6 dB IL.
- Amp: Mini Circuits ZVE-8G+, 35.5 dB gain, 4.1 dB NF.
- Circulator: Ditom D3C3060, 0.2 dB IL.
- Antenna: Schwarzbeck BBHX 9120 LF, 13 dBi gain.

The RF filters provide better than 70 dB IL from DC-3000 and 3600-11500 MHz, an important factor as the design is using direct-RF sampling and signal generation. No mixers are necessary, which reduces the number of components and removes the need for a high quality local oscillator (LO).

The transmitter part of the path has a filter to remove image frequencies, and a set of amplifier stages. There is an RF switch in front of the high power amplifier (HPA) to reduce the noise when the radar is not transmitting; however, the internal noise from the HPA is not removed with this design. A circulator ensures better than 24 dB isolation between transmitter and receiver stages. The output power is 30 dBm, and the antenna provides 13 dBi gain.

The receiver path consist of components of the same make as the transmit path, except of a low noise amplifier (LNA) of model Mini Circuits PSA4-5043+ with 10.2dB gain and 1.1dB NF. An RF switch is used to ensure additional isolation when the transmitter sends a pulse. After the RF switch, a filter and LNA ensures good spectral quality and maximizes the signal-to-noise ratio. Finally, a set of amplifiers is used to put the signal at correct power level for the ADC.

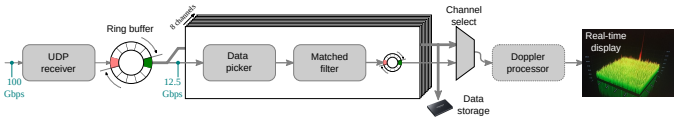

Figure 3. VERA Data Flow. The radar currently transmits data from two channels over 10 Gbps Ethernet, but aims to eventually receive data from eight channels over 100 Gbps Ethernet. Each channel gets assigned a quad-core sharing the same L3-cache. The key challenge is distributing data to each quad-core without hitting the rather limited per-core memory bandwidth.

III. Software

Our processing PC consists of a 32-core AMD Threadripper 3975WX CPU (Zen 2) and an Nvidia RTX 3090. To facilitate high algorithmic flexibility and fast development time, the Threadripper performs all data processing thus far. It provides 11 Gflops per-core processing speed, but only 1.5 GB/s per-core memory bandwidth, which makes memory management critical.

As the data flow in Figure 3 illustrates, the VERA-radar aims to eventually receive data from 8 channels over the 100 Gbps Ethernet link provided by the RFSoC. To allow scaling to this, each channel is granted four unique cores of the Threadripper that make up a ”core complex die” sharing the same L3-cache. The UDP-packets are received in chunks of 8192 bytes, fed into a highly optimized ringbuffer and then read by every channel running on its unique quad-core die. Every channel selects its data, performs matched filtering and stores the result in another ringbuffer. A post-processing thread writes matched filtered data from all channels to disk and optionally performs Doppler processing on a selected channel for a real-time display.

While the design works for our current two channels sharing a 10 Gbps Ethernet link, some improvements are needed to scale to the full-rate eight channel system. For example, the channel data is currently interleaved in the UDP-stream, but 64 bytes should be sent from each channel at a time to fully fit the cache line and improve bandwidth. For more demanding signal processing such as adaptive beamformers, the GPU will likely be used.

The processing PC is configured with Linux, SSH-server and VirtualGL. This allows remotely controlling the radar in the field with higher responsiveness and graphics quality than remote desktop solutions tend to provide. Running the pre-processing on a CPU has the benefit of not requiring more than a fairly decent laptop for collecting data. Perhaps upcoming embedded processors on the RFSoC can do this task on their own, making the post-processing computer entirely optional?

IV. Measurement Results

The VERA radar system has been tested in different configurations in order to explore the versatility of the system. The system consists of two channels with orthogonal polarizations and, hence, it does not support beamforming. However, wideband collection has been tested in three scenarios: wideband dual-pol collection of a vessel, wideband dual-pol collection

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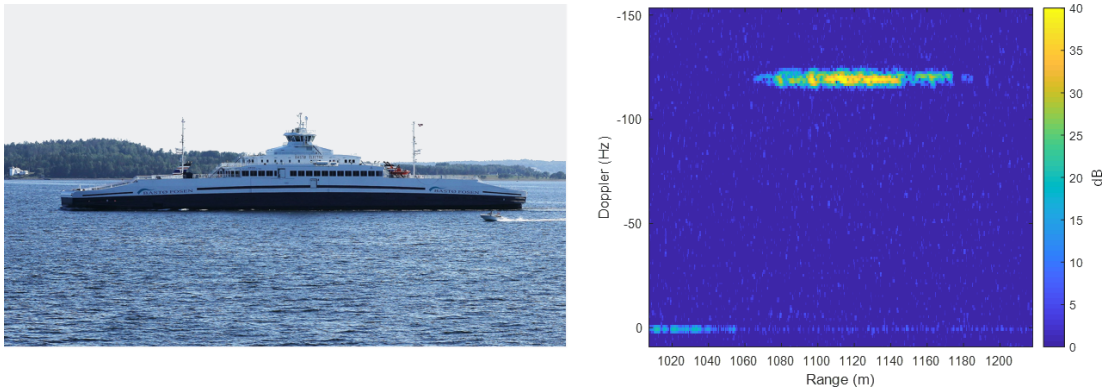

Figure 4. Wideband collection of vessel with the VERA system, showing a range-Doppler plot of the Bastøy 5 vessel with length 143 meters. The vessel is seen partly from behind and, hence, the length can be estimated to at least 130 meters from the plot.

of land target, and dual-band synthetic aperture radar (SAR) collection. The waveform used is a 280 MHz pulse and 2.5 kHz PRI without any stagger.

Figure 4 shows a wideband collection of a vessel. The recording was done at Jeløy, from a beach overlooking a busy ferry-crossing of the Oslo fjord. The vessel is 143 meters long, and is observed at a slightly diagonal course. The range profile is visible in the range-Doppler map at approximately 120 Hz. The processing performed on this dataset is a standard matched filter and Doppler processing of a set of pulses to produce the range-Doppler map.

A dual polarization wideband collection was performed for a land target (car) and is show in Figure 5. The top-left plot shows co-pol (H TX, H RX), top-right plot shows co-pol (V TX, V RX), bottom-left shows cross-pol (H TX, V RX) and bottom-right shows cross-pol (V TX, H RX). Cross-pol plots shows similar results; however, the co-pol plots shows some differences in signature. The system has not been calibrated yet, therefore, the levels could not be compared as of now.

A SAR collection was also performed with the VERA system. In SAR, a baseline is created by moving the antenna over the integration interval. The radar antenna was mounted on the roof of a car, and the baseline was created by driving on a straight road overlooking Kjeller outside Oslo in Norway. In order to generate a focused SAR image, navigation is regularly incorporated into the processing to compensate for deviations from a straight baseline. In this case, no navigation has been used and, hence, the image is not perfectly focused. Other data driven methods could also be applied, such as auto-focus algorithms, to better focus the image. Figure 6 and 7 shows

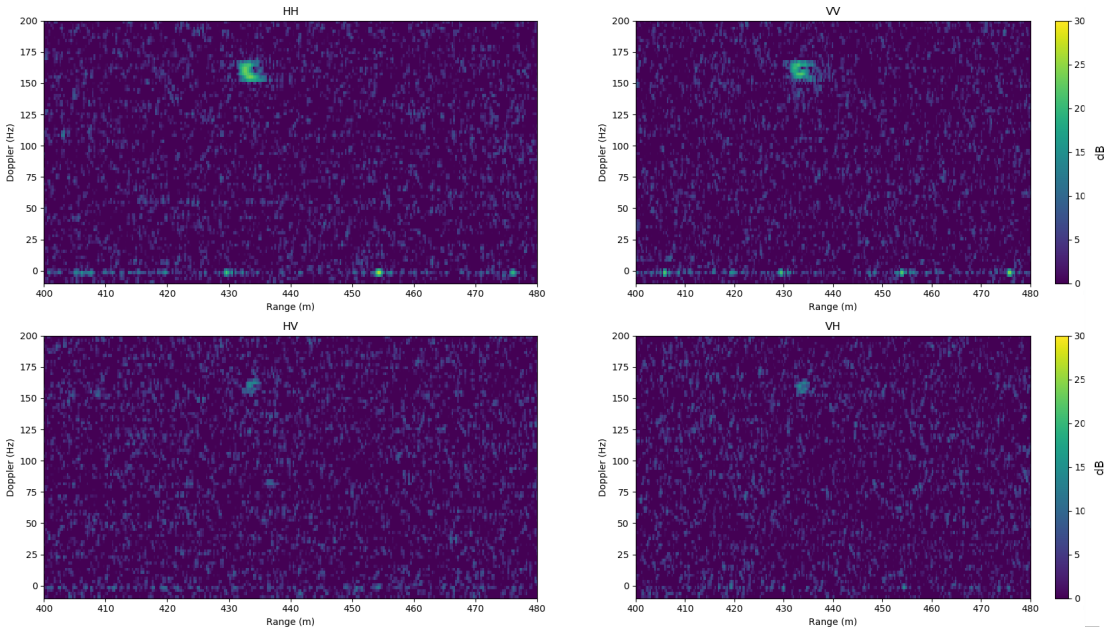

Figure 5. Wideband dual-pol collection of car with the VERA system, showing a range-Doppler plot for co- and cross polarizations. The top-left plot shows co-pol (H TX, H RX), top-right plot shows co-pol (V TX, V RX), bottom-left shows cross-pol (H TX, V RX) and bottom-right shows cross-pol (V TX, H RX). Co-pol signature is slightly different; however, the system is not calibrated and hence the levels cannot be compared as of now.

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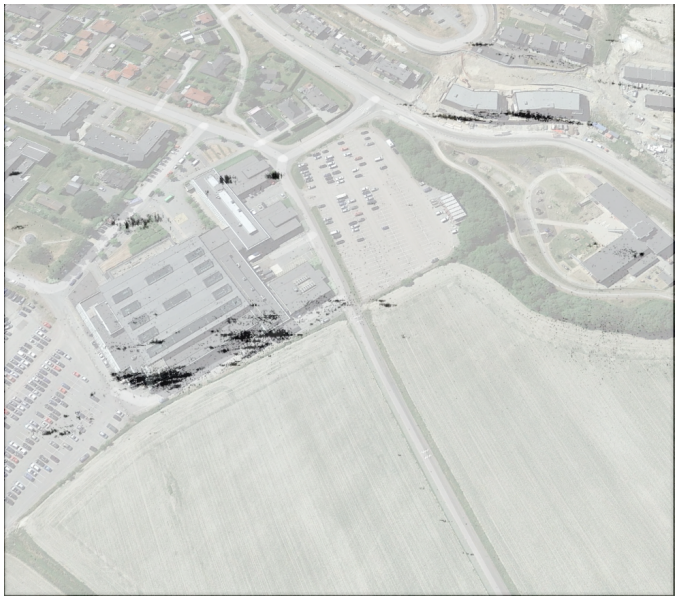

Figure 6. SAR dual-pol collection of area at Kjeller with the VERA system. SAR overlay in Google Earth. Buildings and lamp-posts is visible in the SAR image, amongst other features.

Figure 7. SAR dual-pol collection of other area at Kjeller with the VERA system. SAR overlay in Google Earth. Creek, tree-line and farm building is visible in the SAR-image.

two areas of a SAR image collected with the VERA system. The data was processed using a back-projection algorithm. The dataset used was pre-processed with the same matched filter processing used in the previous examples for vessel and car.

Figure 6 shows a SAR image overlay with a set of buildings, car park and road. Along the road in the right lower part of the image, the reflections of the lamp posts along the road is visible. Building edges matches the buildings in the overlay.

Figure 7 shows a different part of the SAR image, with a farm building, creek with tree-line and some houses. The creek and tree-line is visible in SAR overlay is visible in the top part of the image.

V. Conclusions

This work has shown a dual-pol S-band radar system developed using the Xilinx RFSoC Gen1 chip on the ZCU111 evaluation board. The radar system, called VERA (VErasitle RAdar), consists of evaluation boards and connectorized components for simplicity of the development phase. Measurement results of a sea-going vessel has been shown using a high resolution waveform, and the minimum length of the vessel may be estimated from the measurement. A dual-polarization measurement of a car is performed, and the co- and cross-polarization signatures are shown, with some differences in the horizontal and vertical polarized signatures. Finally, results of an early SAR-measurement from the roof of a vehicle is displayed. The versatility of the VERA system has been shown in this work, where it has been utilized for vessel characterization, dual-pol measurement and SAR imaging.

VI. Future work

The VERA system is a dual-pol system, and must be calibrated in order to do further research on the multi-pol properties of different targets. Dual-pol calibration, both relative and absolute, is an important first step for further work.

The design of the VERA system has been the start from the radar group at FFI for developing multifunction RF systems on the RFSoC platform. The radar has shown promising results by itself, and the radar design alone is using a sparse amount of the resources of the FPGA. A natural progress of the work will be to incorporate also other systems like ES to enhance situational awareness.

The VERA has little flexibility in its current state, where many parameters are hard-coded into the FPGA bitfile. The design will be developed into a more dynamic system where the radar parameters can be changed in real-time on the FPGA. Working together with an ES system, this could for example result in changing the radar parameters to mitigate interference.

Digital beamforming has been a topic of research at FFI, especially to suppress and mitigate interference into radar receivers. Developing the radar into a functional multi-channel system to enable digital beamforming will be at the focus of research, and the new 3rd generation RFSoC's with their 16 channel systems is therefore a natural system to focus the development onto. Together with this, real-time wide bandwidth digital beamforming on the FPGA need to also be developed.

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